Design and Simulation Reversible TSG Gate For Application of Efficient Adder Circuits

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Abstract

In the recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology, and optical computing. The classical set of gates such as AND, OR, and EXOR are not reversible. This paper proposes a new 4 * 4 reversible gate called "TSG" gate. The proposed gate is used to design efficient adder units. The most significant aspect of the proposed gate is that it can work singly as a reversible full adder i.e reversible full adder can now be implemented with a single gate only. The proposed gate is then used to design reversible ripple carry and carry skip adders. It is demonstrated that the adder architectures designed using the proposed gate are much better and optimized, compared to their existing counterparts in literature; in terms of number of reversible gates and garbage outputs. Result of simulated circuit shown in this paper. Thus, this paper provides the initial threshold to building of more complex system which can execute more complicated operations using reversible logic.

Keyword : *adder, reversible,* TSG *gates, carry*

1. Introduction

Researchers like Landauer have shown that for irreversible logic computations, each bit of information lost, generates kTlog2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [12]. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information. Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa. In the reversible circuits, there is a one-to-one mapping between input and output vectors. Bennett's theorem [2] about heat dissipation is only a necessary and not sufficient condition, but its extreme importance lies in the fact that every future technology will have to use reversible gates to reduce power. As the Moore's law continues to hold, the processing power doubles every 18 months. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit. The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low-power CMOS design, optical computing, nanotechnology and quantum computing. The most prominent application of reversible logic lies in quantum computers. A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; each gate performing an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information; corresponding to the classical bit values 0 and 1. Any unitary operation is reversible hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).Thus, Quantum Arithmetic must be built from reversible logical components [14].

One of the main constraints in reversible logic is to minimize the number of reversible gates used and garbage output produced. Garbage output refers to the output that is not used for further computations. In other words, it is not used as a primary output or as an input to other gate. In literature, there are a number of existing reversible gates such as Fredkin gate[3,13,1],Toffoli Gate[3,13] and New Gate[11]. In this paper, the focus is on the proposal of new reversible 4*4 TSG gate. The proposed TSG gate is used to design optimized adder architectures like ripple carry adder and carry skip adder. It has been proved that the adder architectures using the proposed TSG gate are better than the existing one in literature; in terms of number of reversible gates and garbage outputs. Thus, the paper provides the initial threshold to build more complex systems which can which can execute

more complicated operations. The reversible circuits designed and proposed here form the basis of the ALU of a primitive quantum CPU[7,8,9].

2. Proposed 4*4 Reversible Gate

In this paper, a 4 * 4 one through reversible gate called TS gate "TSG" is proposed. The proposed reversible TSG gate is shown in Fig. 1. The corresponding truth table of the gate is shown in Table 1. It can be verified from the Truth Table that the input pattern corresponding to a particular output pattern can be uniquely determined. The proposed TSG gate can implement all Boolean functions. Fig. 3 shows the implementation of the proposed gate as XOR function. Fig. 2 and Fig. 4 shows the implementation of the proposed gate as NOT and NOR function respectively.

Table 1. Truth table of the propsed TSG Gate

a. Input binary

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

b. Output TSG

P	Q	R	S
0	0	0	0
0	0	1	0
0	1	1	1
0	1	0	0
0	1	1	0
0	1	0	1
0	0	0	1
0	0	1	1
1	1	1	0
1	1	0	1
1	1	1	1
1	1	0	0
1	0	0	1
1	0	1	1
1	0	0	0
1	0	1	0

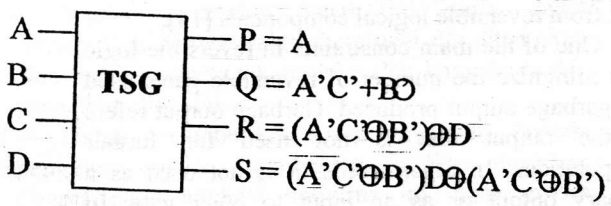

Figure1. Proposed Reversible TSG Gate

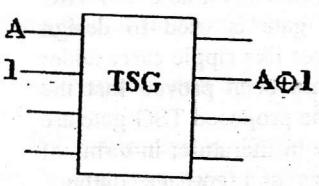

Figure 2. Proposed TSG Gate as NOT Gate

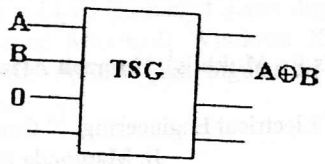

Figure 3. Proposed TSG Gate as XOR Gate

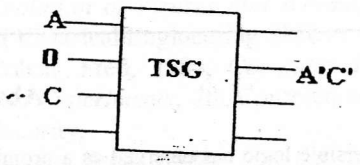

Figure 4. Proposed TSG Gate as NOR Gate

A number of reversible full adders were proposed in [4,5,6,10,11]. The reversible full adder circuit in [14] requires three reversible gates (two 3*3 new gate and one 2*2 Feynman gate) and produces three garbage outputs. The reversible full adder circuit in [4,5] requires three reversible gates (one 3*3 new gate, one 3*3 Toffoli gate and one 2*2 Feynman gate) and produces two garbage outputs. The design in [10] requires five reversible Fredkin gate and produces five garbage outputs. The proposed full adder using TSG in Fig. 5 requires only one reversible gate (one TSG gate) and produces only two garbage outputs. Hence, the full-adder design in Fig. 5 using TSG gate is better than the previous full-adder designs of [4,5,6,10,11]. A comparative result is shown in Table 2

Table 2. Comparative Result of Different Full Adder Circuit

	No. of gates	No. off garbage output
Proposed Circuit	1	2
Existing Circuit[6]	3	3
Existing Circuit [7,8]	3	2
Existing Circuit [9]	5	5

3. Application and Simulation of Proposed TSG Gate.

To illustrate the application of the proposed TSG gate, two different types of adders – ripple carry and carry skip adders are designed. It has been proved that the adders circuit drawn using the proposed gate are the most optimized one compared to their existing counterparts in literature.

3.1. Ripple Carry Adder

The full adder is the basic building block in the ripple carry adder. The full adder circuit using the proposed TSG gate is shown in Fig. 6. The ripple carry adder is obtained by cascading the full adders

in series. The output expressions for a ripple carry adder are : Si= A⊕B⊕Ci;
Ci+1=(A⊕B).Ci⊕AB, (i=0,1,2....)

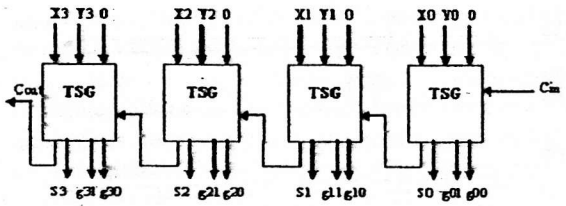

Figure 6. Ripple Carry Adder using the proposed TSG Gate

It can be inferred, from the Fig. 6 that for N bit addition; the proposed ripple carry adder architecture uses only N reversible gates and produces only 2N garbage outputs. There also exists previously proposed ripple carry adders in the literature. But, the ripple carry adder using our proposed TSG gate is the most optimized one. Table 3 shows the result that compares the proposed ripple carry adder using TSG gate, with the existing full adders of [4,5,6,10,11]. It is observed that the proposed circuit is better than the existing circuits; both in number of reversible gates and garbage outputs.

Table3. Comparative result of different ripple carry adder circuits

	No. of gates	No. off garbage output
Proposed Circuit	N	2N
Existing Circuit[6]	3N	3N
Existing Circuit [7,8]	3N	2N
Existing Circuit [9]	5N	5N

3.2. Carry skip Adder

In the carry skip adder, delay is reduced due to the carry computation. In the full adder operation, if either input is a logical one, the cell will propagate the carry input to its carry output. Hence, the ith full adder carry input Ci, will propagate to its carry output, Ci+1, when Pi= Xi⊕Yi. In addition, the multiple full adders, making a block can generate a "block" propagate signal P to detour the incoming carry around to the block's carry output signal. Fig. 7 shows a four bit carry skip adder block. It is quickly determined by each block, that whether the block's carry input is propagated to its carry output. If the block propagate P is one, the block carry input Cin is propagated as the block carry output Cout. An AND gate is used to generate a block propagate signal P. Fig. 9 shows the proposed carry skip compatible Full adder constructed with TSG gate.

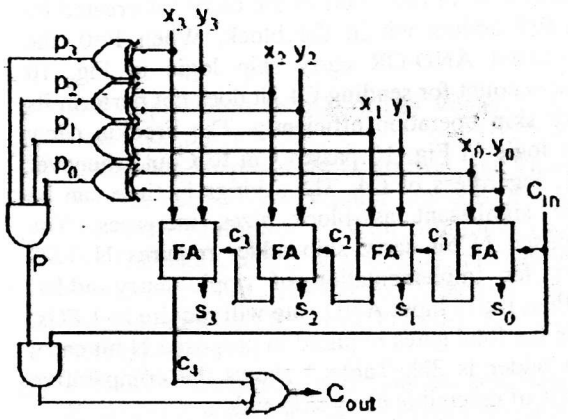

Figure 7. Four bit skip adder block

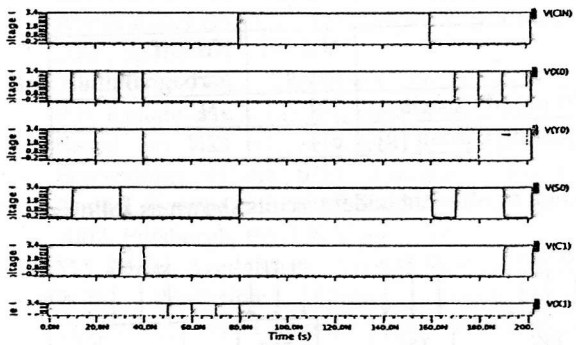

Figure 8. Result of one bit full adder simulation.

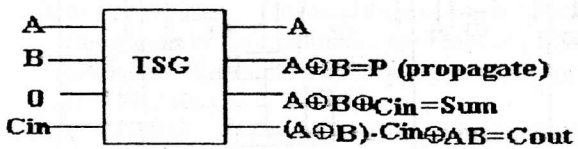

Figure 9. Full adder circuit (with propagate) using TSG Gate

The conventional skip block in Fig. 7 uses the AND-OR gate combination. Fig. 9 shows the block diagram of the carry skip adder block constructed with TSG gates and Fredkin gates (FG). The three FGs in the middle of Fig. 10 are used to perform the AND4 operation. This will generate the block propagate signal P. The single FG in the left side of Fig. 10 performs the AND-OR function to create the carry skip logic and generate the block carry out signal Cout. Inthe proposed carry Skip adder, the FG propagates theblock's carry input to the next block if the block propagate signal P is one; otherwise, the most significant full adder carry C4 is propagated to the next block. The traditional carry skip AND-OR logic in Fig. 7 and the carry skip logic in Fig. 10 do not have the equivalent truth Tables but itmust be noted that the Fredkin carry skip logic morefaithfully adheres to the spirit of carry skip addition by propagating the correct value of Cin to Cout. The FG carryskip logic in Fig. 10 can lead to improve carry propagation,when the block carry propagate signal P is one. When P is one, the block

carry input Cin must propagate to the next block, independent of the result of the carry C4 created by the full adders within the block. When P=0, the traditional AND-OR carry skip logic in Fig. 10 must account for sending C4 , it does not perform its carry skip operation efficiently. The Fredkin carry skip logic in Fig. 10 passes Cin to Cout whenever P=1, regardless of C4. The savings in time can be quite significant as block sizes increases. The proposed N bit carry skip adder requires N TSG gates for implementation of ripple carry adder. Further, the N input AND gate will require N-1 FGs. Thus the total gates required in proposed N bit carry save adder is 2N. Table 4 shows the comparative results of reversible carry skip adders.

Table 4. Comparative results of different reversible carry skip adder circuits

	No. of gates	No. off garbage output
Proposed Circuit	2N	3N
Existing Circuit [9]	6N	12N

Design of efficient adder circuits shown as follows :

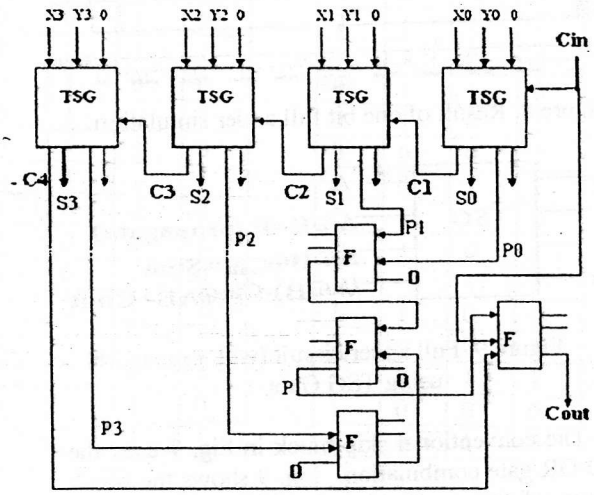

Figure 10. Four bit carry skip adder block using proposed TSG and Fredkin (F) gates.

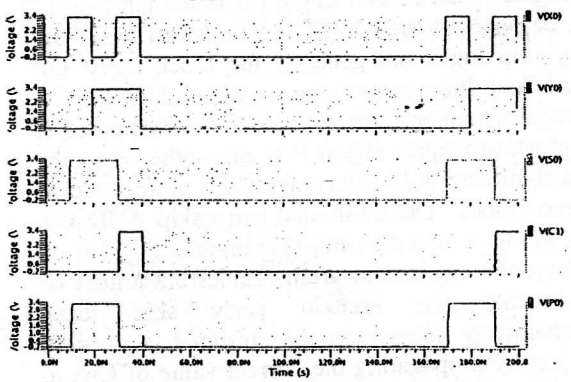

Figure 10a. Result of TSG1 Simulated

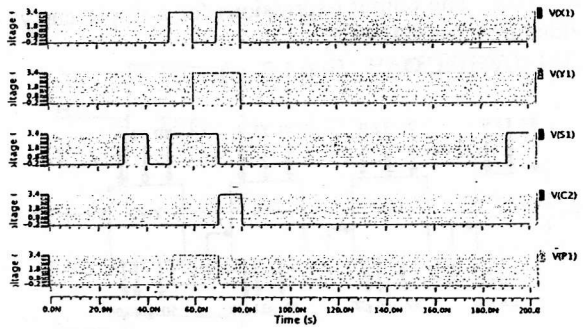

Figure 10b. Result of TSG2 simulated

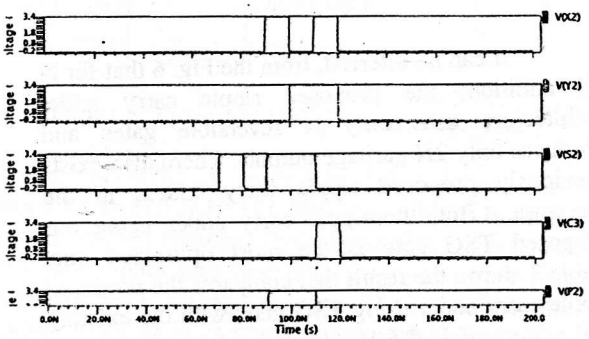

Figure 10c. Result of TSG3 simulated

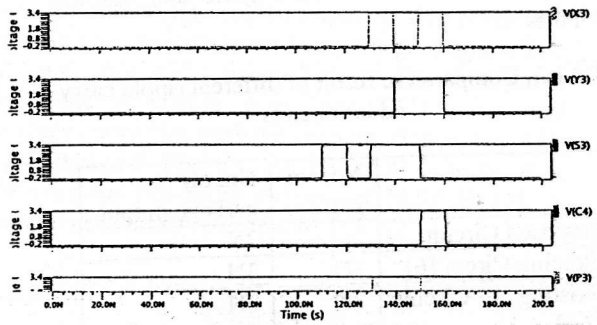

Figure 10d. Result of TSG4 simulated

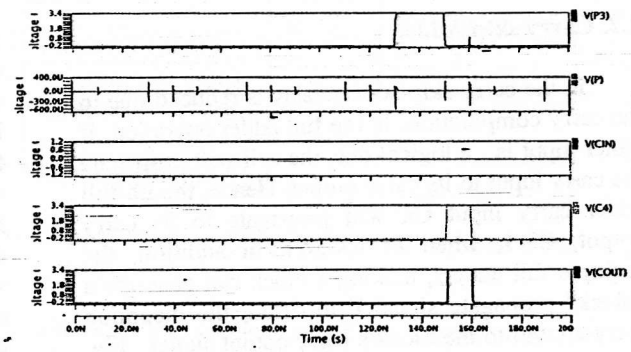

Figure 10e. Result of propagation simulatied

4. Conclusions

The focus of this paper is the proposal of new reversible 4*4 TSG gate. The proposed TSG gate is being used to design optimized architectures of ripple carry and carry skip adders. It is proved that the adder architectures using the proposed TSG gate

are better than the existing counterparts in literature, in terms of number of reversible gates and garbage outputs. All the proposed architectures are analyzed in terms of technology independent implementations. The technology independent analysis is necessary since quantum or optical logic implementations are not available. There are a number of significant applications of reversible logics such as low power CMOS, quantum computing, nanotechnology, and optical computing and the proposed TSG gate and efficient adder architectures are one of the contributions to reversible logic. The proposed circuit can be used to design large reversible systems. In a nutshell, the advent of reversible logic will significantly contribute in reducing the power consumption. Thus, the paper provides the initial threshold to build more complex systems which can which can execute more complicated operations. The reversible circuits designed and proposed here form the basis of the ALU of a primitive quantum CPU.

5. References

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